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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,085	02/03/2004	Chad A. Cobbley	MICS:0078-3	1967

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Michael G. Fletcher
Fletcher Yoder
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,085	COBBLEY ET AL.	
	Examiner	Art Unit	
	David S Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 and 8-20 is/are rejected.

7)☒ Claim(s) 2-7 is/are objected to.

8)☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 03 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/3/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the application filed 2/3/04.

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: Claim 17 recites forming a "shingle stack". It is believed the applicant meant "single stack".. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 9-11, 15, 18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Blackshear (US006774475B2).

Blackshear teaches all of the positive steps of claims 1, 9-11, 15, 18, and 20 in that a stack of at least two semiconductor die are formed (column 4 lines 8-9), and the stack is tested prior to mounting on a packaging substrate (claim 14).

Regarding claim 9, Blackshear tests for defective chips (column 4 lines 10-11), thus functionally testing.

Regarding claim 10, Blackshear tests for data pins (column 4 lines 37-39), thus environmentally testing.

Regarding claim 11, as the stack is tested prior to mounting on a packaging substrate (claim 14) it must be attached to a package substrate. electrically connecting the stack is coupling.

Regarding claim 15, the packaging substrate comprises a wafer (120, substrate is a wafer).

Regarding claim 18, the tested stack package forms an integrated circuit (IC) package (column 1 line 49).

Regarding claim 20, the stacked die comprises a memory die (column 1 lines 22-23).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 12-13, 16-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang (US 6,343,019) in view of Blackshear (US006774475B2) and Pai (US 6503776).

Jiang teaches all of the positive steps of claims 8, 12-13, 16-17, and 19 as recited above, except for testing the stack prior to mounting on a packaging substrate and that a stack may be three or more chips.

Blackshear teaches a stack of at least two semiconductor die are formed (column 4 lines 8-9), and the stack is tested prior to mounting on a packaging substrate (claim 14). The pre-testing is done to reduce rework or discard of packages (column 4 lines 10-15).

Regarding claim 8 Jiang teaches stacking two semiconductor die, but also "the present invention can be applied to other geometry die and die arrangements". This is suggestive of three or more die in the stack. Pai teaches a die stack comprising three (110, 160, and 130) die. Pai teaches multi-chip modules help minimize the system operational speed restrictions imposed by long printed circuits (column 1 lines 16-18).

Regarding claim 12, the stack may be formed (or secured to the substrate) by the use of adhesive tape (Jiang, column 3 line 62), thus a tape reel.

Regarding claim 13, the adhesive of Pai may be a film adhesive, thus the stack is placed upon a film frame (column 4 lines 2).

Regarding claim 16, Pai teaches when using adhesive in a multi-stack, the second adhesive should have a lower curing temperature (exothermic temperature) than that of the first adhesive (column 3 lines 29-37).

Regarding claim 17, the stack is a single stack (Jiang, figure 6).

Regarding claim 19, Pai teaches that it is known to use stacked chips in connection with processors (thus forming an electronic system) to minimize the system operational speed restrictions imposed by long printed circuits (column 1 lines 16-19).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Jiang by pre-testing the stack prior to package mounting to reduce rework or discard of packages (column 4 lines 10-15) and to use at least three chips in a stack as taught by Pai to help minimize the system operational speed restrictions imposed by long printed circuits (column 1 lines 16-18).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang (US 6,343,019) in view of Blackshear (US006774475B2) and Moden (US 5719440) or Hakey (US006627477B1).

Jiang and Blackshear teach all of the positive steps of claim 14 as recited above except for using a gel. Jiang teaches an adhesive or adhesive tape. Moden teaches bonding "to an upper surface of a master board with an adhesive, which may comprise a liquid or gel adhesive, or an adhesive tape, all as known in the art." (column 4 lines 46-49) Thus the three have art recognized equivalence. Hakey uses a polyimide with a solvent (a gel) to bond chips (column 3 lines 22-35).

It would be obvious to one skilled in the requisite art at the time of the invention to modify Jiang and Blackshear by using a gel as taught by Hakey and by Modem to be known in the art, and to be an art recognized equivalence.

Allowable Subject Matter

7. Claims 2-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 contains the limitation of stacking semiconductor die where a first die is picked and held by the apparatus, an adhesive is applied to a surface and while being held by the apparatus, and a second die is placed on the adhesive layer to form the die stack. This limitation, in combination with the other limitations of claim 2 is not taught or suggested by the prior art of record. Pai (US006503776B2 and US006387728B1) forms the stack by first bonding a die to a substrate and then bonding a die to the first die.

Thus, the first die is not held by a pick-apparatus when the second die is bonded (stacked). Rajagopalan (US006586825B1) also stacks the die in place on the substrate.

Claims 3-7 are dependent upon objected claim 2.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

September 7, 2004